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Layout Design of a 2-bit Binary Parallel Ripple Carry Adder Using CMOS NAND Gates with Microwind

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Abstract

A good deal of ingenuity can be exercised and a vast amount of time wasted exploring layout topologies to minimize the size of a gate or other circuitry such as an adder or memory element in an integrated circuit. This paper represents a simple and compact layout design for two bit binary parallel ripple carry adder using only CMOS NAND gates with the help of Microwind as a tool for design and simulation. Construction of this adder for fabricating involves the design of 2-input, 3-input, 4-input NAND gates and CMOS NAND inverters. The performance parameters are analyzed from the simulation responses and characteristics curves of the proposed design. The optimization of the design towards single P^+ or N^+ diffusion, single $+V_{dd}$ and single $-V_{dd}$ supply contributed to lesser area and improved functionality of the adder circuits performance.

I. Introduction

The trend of CMOS (**C**omplementary **S**ymmetry **M**etal **O**xide **S**emiconductor) technology improvement continues to be driven by the need to integrate more functions within a given silicon area, reduce the fabrication cost, increase operating speed and dissipate less power. Past few years have seen the introduction of nano-scale technologies for industrial production of high performance integrated circuits (IC). [1] Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. [2, 3, 4, 5]

Microwind is a CMOS circuit editor and simulation tool for logic and layout-level design, running on Microsoft Windows. It has been developed since 1998 through several versions, and is available as a freeware (lite version [6]) for educational purpose. In this paper, a 2-bit binary parallel adder based on CMOS NAND gate layout is designed using Microwind 3.1. First of all the individual components, the NAND inverter, 2-input, 3-input and 4-input NAND gates were designed, aligned and connected properly. The overall design diagram, 3D view of the layout and performance graphs are presented for a greater understanding.

II. Background Theory

A full adder circuit is used to add A_n, B_n and C_{n-1} where A_n and B_n are the nth order bits of the numbers A and B respectively and C_{n-1} is the carry generated from the addition of (n-1)th order bits. Table 1 shows the truth table and figure 1 shows the logic diagram of a 1-bit full adder. Logical circuit using multiple full adders to add N-bit numbers can be created. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. This kind of adder is a *ripple carry adder*, since each carry bit "ripples" to the next full adder.

Table. 1. Truth table of a 1-bit full adder

Inputs			*Outputs*	
A_n	B_n	C_{n-1}	S_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum, $S_n = H_K \cdot \overline{C_{k-1}} + \overline{H_k} \cdot C_{k-1}$

New Carry, $C_k = A_k \cdot B_k + H_k \cdot C_{k-1}$

Where, half sum, $H_k = \overline{A_k \oplus B_k}$

$= \overline{A_k} \cdot B_k + A_k \cdot \overline{B_k}$

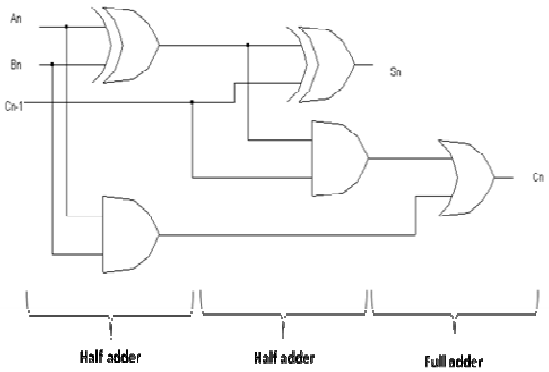


Fig. 1. Logic diagram of a 1-bit full adder

The formation of a 2-bit full adder using two 1-bit adders is illustrated in figure 2.

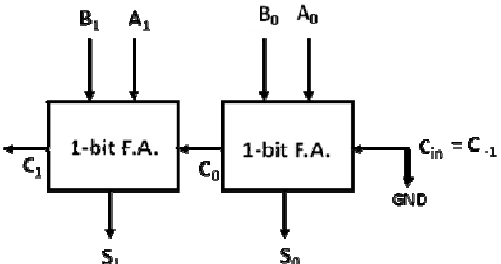


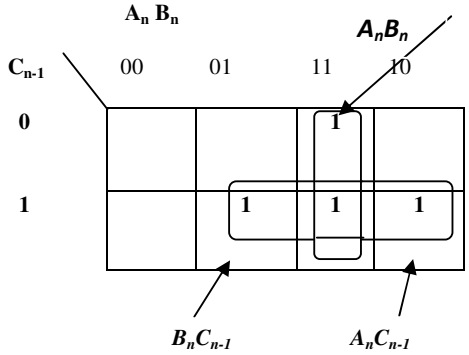
Fig. 2. 2-bit full adder block diagram

he K-maps for the outputs S_n and C_n are shown in table 2 and table 3 respectively.

Table. 2. K-map for S_n

C_{n-1} \ $A_n B_n$	00	01	11	10
0		1		1
1	1		1	

Table. 3. K-map for C_n



Therefore the minimized Boolean Expression for S_n and C_n will be as expressed in Eqn. 1a. and Eqn. 1b.

$$S_n = \overline{A}_n B_n \overline{C}_{n-1} + \overline{A}_n \overline{B}_n C_{n-1} + A_n \overline{B}_n \overline{C}_{n-1} + A_n B_n C_{n-1} \quad (Eqn.1a)$$

$$C_n = A_n B_n + B_n C_{n-1} + A_n C_{n-1} \quad (Eqn.1b)$$

Finally the NAND realization of Sum bit and Carry bit based on the minimized expression is illustrated in figure 3. [7, 8, 9]

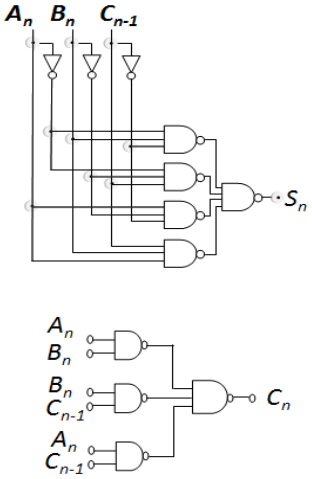


Fig. 3. NAND realization of S_n and C_n for binary Adder

III. Design of the Adder

The design of a 2-bit binary parallel adder involved the design of CMOS NAND inverters, 2-input NAND gates, 3-input NAND gates and 4-input NAND gates. Finally these components were arranged and necessary interconnections were established to perform the specified logical operation.

Realization of a CMOS NAND inverter

This inverter is designed using a 2-input CMOS NAND gate shown in figure. The 2 inputs are shorted to obtain inverted output. The two parallel PMOS gates are designed in a single P+ diffusion region. The design is developed using 250nm standard fabrication technology. The gate length and width are 2λ and 6λ respectively where λ is the measure of linear distance between the dots shown in fig 4 -8. There are provisions for applying input signal at either side of the Polysilicon. This is for the simplicity of the overall design.

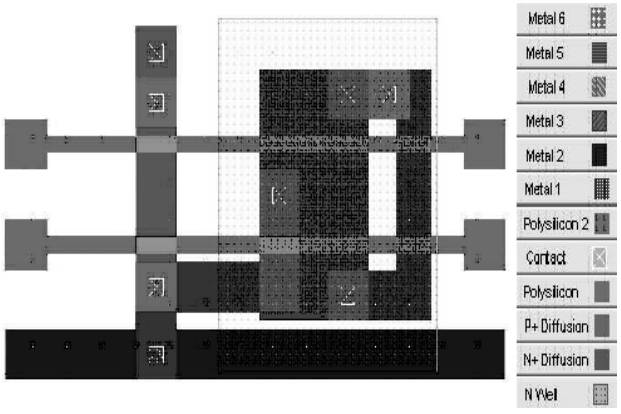


Fig. 4. CMOS NAND inverter

Realization of a 2-input CMOS NAND gate

Figure 5 shows the realization of a 2-input CMOS NAND gate. This is same as the design in figure 4 except the two separate input nodes. This design also provides options for applying input signals and obtaining the output signal from either side. The gate lengths (2λ) are kept very short and widths (6λ) are kept high enough to obtain the rise time and fall time sufficiently small. The output is taken out using metal layer 2 to avoid unnecessary interconnections.

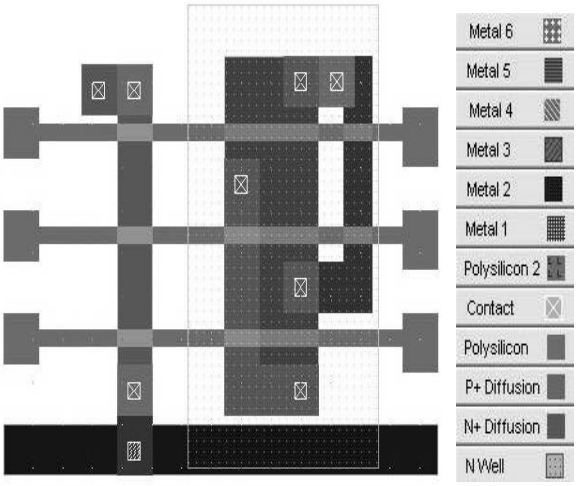


Fig. 5. 2-input CMOS NAND gate

Realization of a 3-input CMOS NAND gate

The 3-input CMOS NAND gate shown in figure 6 is designed exactly the same way as the 2-input NAND gate in figure 5. The parallel PMOS gates are located in a single P+ diffusion layer. This design excludes the use of extra Polysilicon as used in conventional design layout.

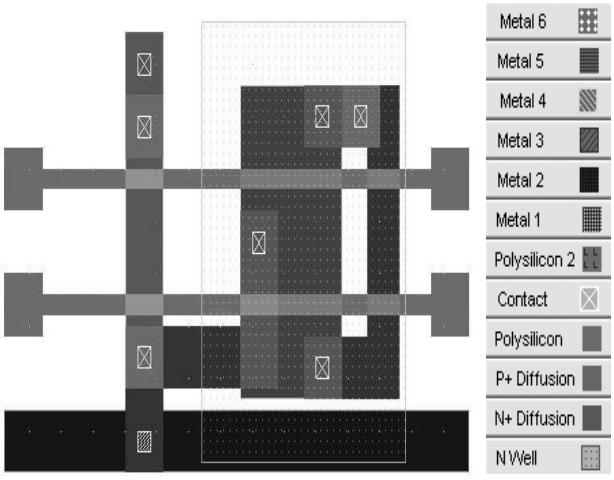


Fig. 6. 3-input CMOS NAND gate

Realization of a 4-input CMOS NAND gate

The 4-input CMOS NAND gate presented in figure 7 is also designed exactly the same way as the designs in figure 4, figure 5 and figure 6. Use of single P+ diffusion layer contributed towards elimination of redundant Polysilicon.

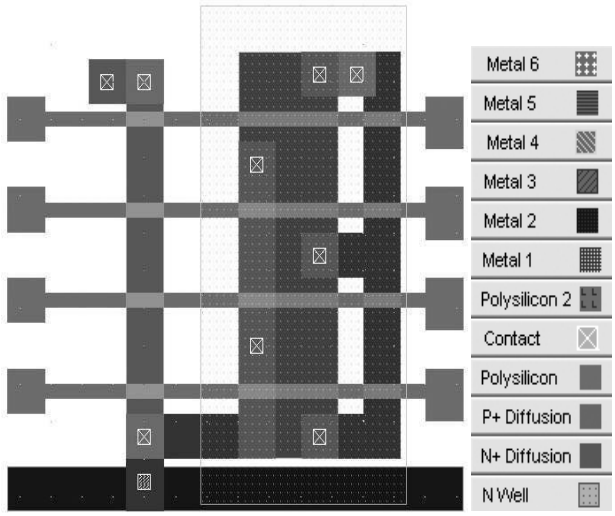


Fig. 7. 4-input CMOS NAND gate

Final layout of 2-bit NAND Adder

When all the 4 types of logic gates were designed they were simply copied and pasted side by side in such a way as to resemble the figure 1 to design a 1 bit full adder. The 3 (2 binary bits and a carry bit) input signals were fed from a horizontal metallic bus line at the top of the design into 3 CMOS inverters. The inverted outputs were also available at 3 different bus lines. At this stage the necessary interconnections were achieved carefully in a regular fashion. The whole 1 bit full adder was copied and pasted side by side to form a 2 bit adder. The final design was optimized to form single P+ diffusion, single $+V_{dd}$ and single $-V_{ss}$ supply. Figure 8 shows the final diagram and figure 9 represents the end of the process 3D architecture of the designed layout.

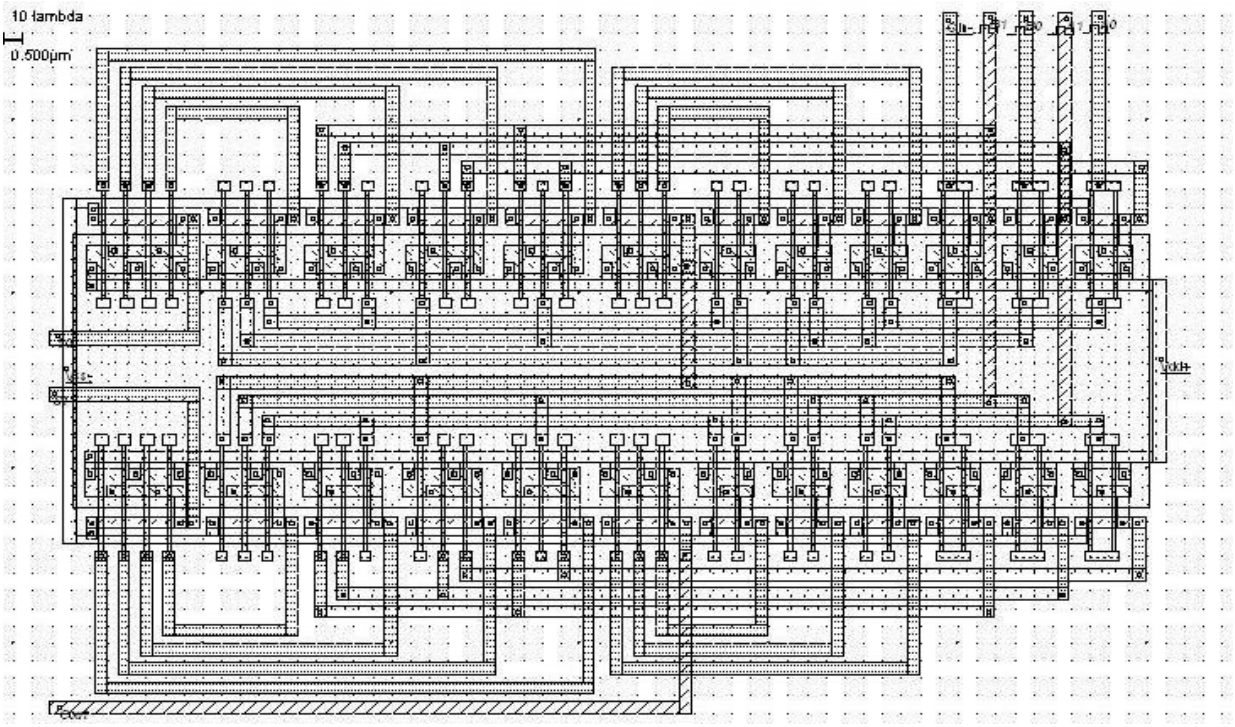


Fig. 8. Final formation of the NAND Adder

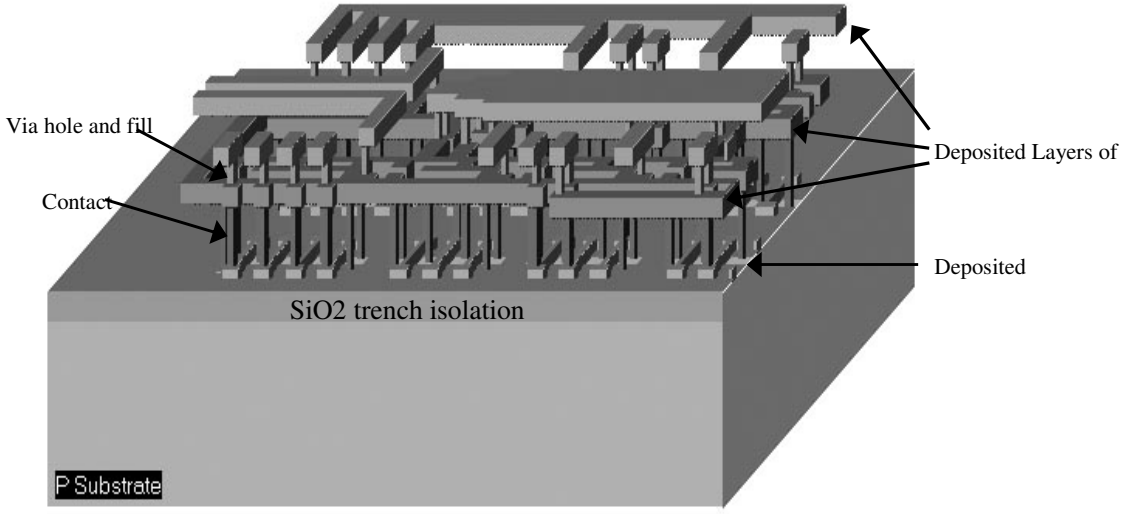


Fig. 9. 3D view of the designed layout

Figure 9 shows the 3D view of the designed layout. The design involved the steps of Substrate preparation, N diffusion, SiO_2 trench isolation, Polysilicon deposition, N+ and P+ implantation, creating metal contacts, 3 layers of metal deposition, etching, and respective via hole filling.

IV. Performance of the Adder

CMOS logic dissipates less power than any other logic circuits. This is because CMOS dissipates power only when switching ("dynamic power"). On the other hand, NMOS logic dissipates power whenever the output is low ("static power"), because there is a current path from Vdd to Vss through the load resistor and the n-type network [10]. The performance parameters of the design comes from the direct comparison of CMOS or TTL family gates, listed at table 4.

Table. 4. Performance Comparison between CMOS and TTL family [11]

Parameters	CMOS	TTL
Supply	$(V_{DS} - V_{DS}) - 3V$ to 16V	VCC – 5V±0.25
Noise Margin ($V_{min} - V_{max}$ at 1s and 0s)	0.33 and 0 times	0.8V at 0 and 3.8V at 1
Power Dissipation	Only during 1 to 0 or 0 to 1 transition	Continuous
Power Dissipation (dc state)	Very Low	High
Speed	Comparatively low	High

The response curve of the designed NAND Adder was simulated using the same environment and the voltage vs. time response graph is shown in figure 10.

For simulation clock type inputs with frequencies low enough to allow the output to settle were used since this is a ripple carry adder.

The output waveforms of CMOS NAND adder show that the highest delay of output bit S_1 to settle to valid output state is 674ps. So this delay determines the speed of the NAND adder. The performance parameters deduced from the graph and design layout are summarized below.

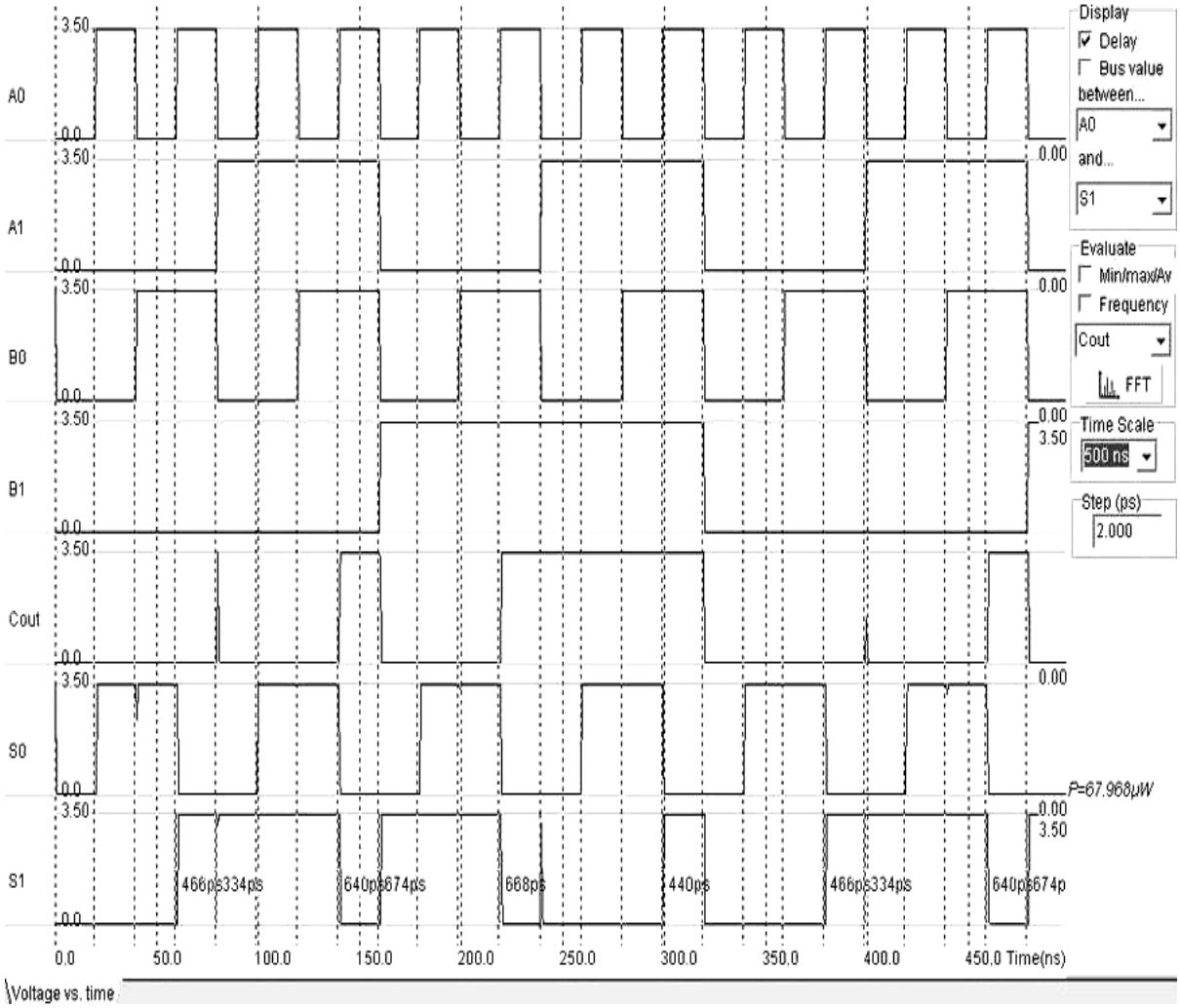
Speed of the NAND adder = $(0.4ns+0.4ns)^{-1}$ = 1.25 GHz.

Highest delay of the adder = 674ps

Average delay of the adder = (321ps + 674ps + 402ps + 387ps + 371ps) / 5= 431ps

Length of the adder = (60 X .5) µm = 30 µm

Width of the adder = (40 X .5) µm = 20 µm



V. Conclusion

This paper presents a basic and compact formation of a 2-bit binary parallel adder using only CMOS NAND gates. Improvement of this layout is possible by designing the gate lengths and widths using more optimization factors. The ripple carry adders are generally slower than other types of adder since the output waits until the carry is generated from previous blocks. The other types of adders such as Carry Select adder, Carry Skip Adder, Carry look ahead adder etc. often require more area than the ripple carry adder. That's why there is always a scope to tradeoff between the speed and the size of the device while designing any adder circuit.

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