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Design of a High Performance Low Cost IC Tester-A Conceptual View

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Abstract

With the improvement of integration technology, complexity of Integrated Circuit (IC) is increasing day by day. The test of such circuit has become a challenge, since it ensures the reliability of electronic products and impacts upon the quality. Conventional IC tester, ATE (Automatic Test Equipment) suffers from serious drawbacks and point towards having a new approach for its economic solution with reliable performance in respect to storage requirement, test application time and fault coverage. In this paper the conceptual design of a high performance low cost IC tester have been proposed. Different test technologies and pattern generator have been reviewed and shown that mixed-mode approach with GLFSR as a pattern generator outperforms all other existing test technologies. In designing of the proposed IC tester GLFSR based mixed-mode approach has been incorporated. It is expected that GLFSR based mixed-mode technique will alleviate the problem of ATE and enhance the performance of the IC tester.

Keywords: ATE, CUT, IC, GLFSR, and SoC

1. Introduction

In this modern era electronic products have become a part of our daily life. The main components of such products are Integrated Circuits (ICs). In IC manufacturing, various physical defects may occur during the numerous physical, chemical and thermal processes [1]. With the dramatic improvement and refinement of integration technology, the design densities and associated complexities of Integrated Circuit (IC) are rapidly increasing. All the functionalities of an electronic system are being integrated on a single chip in less than 2 cm square silicon area. It is expected that this growth will continue in full force in the future years [2]. With this increase in design densities and complexities in IC, the problems of Very Large Scale Integrated (VLSI) circuit testing have become much more acute and complex. The test of such circuit has become a challenge, since it ensures the reliability of electronic products and impacts upon the quality. The cost of testing increases significantly with the complexity of these circuits. It is predicted in a survey that it will soon cost more to test a transistor than to make it. [3]. Testing has now become a major business issues in the production of electronic goods.

The Modern production facilities use computer controlled Automatic Test Equipment (ATE) for testing IC that suffers from the number of serious drawbacks such as high equipment cost, slow test speed, huge memory space to store and to process test data, and yield loss due to inaccuracy of ATE [4]. These drawbacks of ATE are pointing towards having a new approach for testing VLSI circuit. ATE is adopted with D-algorithm which is an idea of 1960's when IC were simple. To alleviate the problems of ATE based IC testing approach, research work is prevalent since 1970. Exhaustive approach [5] offers 100% fault coverage with low computational cost but it is impractical for a complete VLSI chip that has higher number of inputs (e.g. >20) because large number of inputs lead very long test length and longer time for test generation. Pseudo-exhaustive approach [6-7], tests circuit exhaustively by much fewer test vectors than that of the exhaustive approach but hardware implementation of pseudo-exhaustive pattern generator is difficult and most of the design does not lead to minimal test set. Pseudo-random testing approach [8], use simple random pattern generation circuit and a large number test can be generated using smaller data storage within a short period of time. The disadvantage of this approach is the length of the test set that detects a set of faults is much larger than a deterministically generated test set for the same fault. Another implication of this approach is that there are faults in some circuit known as random pattern resistant faults where acceptable fault coverage cannot be achieved even after applying a large number of test patterns. Test processor ASIC design for low cost IC testing, employing weighted random approach has been reported [9-10]. Linear Feedback Shift Register (LFSR) or Cellular Automata Register (CAR) has been used in the research work. Generated patetrns are biased to improve the fault coverage. Later on mixed-mode approach implementing LFSR based pattern generator has been proposed and claimed that this approach outperforms all other test technologies. It ensures complete fault coverage with reduced storage requirements, shorter test application time, and smaller area overhead compared to other approaches [11-13]. Researchers have shown the effetiveness of mixed-mode approach in the Built-in Self-Test (BIST) environment, which is specific to a particular circuit.

In this paper, a general pupose IC tester implementing GLFSR based mixed-mode approach has been proposed for external testing of IC. Since the development of the proposed IC tester is in progress, it is named a conceptual IC tester. The remainder of this paper is organized as follows. Section 2 starts with the concept of redesigning technique, section 3 then presents the proposed IC tester. Next section 4 explores test procedures, finally the paper ends with conclusion in section5.

II. Concept of Redesigning Technique

Mixed-mode Approach

Mixed-mode Technique is a hybrid test technique where deterministic test technique is followed by pseudo-random test technique. This approach exploits advantages of both the pseudo-random test technique and deterministic test

technique. A generalized scheme of mixed-mode technique is shown in Figure 1. Generally most of the faults in a typical circuit are Easy To Detect (ETD), which can be easily detected using first few PRVs and the remaining faults are Hard To Detect (HTD), which need long PRV sequences to detect. In the conventional mixed-mode approach, PRV is generated using LFSR and is applied to a Circuit Under Test (CUT) to detect all the ETD faults and then deterministic test sets are generated using the same LFSR to target the remaining HTD faults using compacted test data named seed. Thereby all the faults of a circuit are detected in mixed-mode approach. This approach ensures complete fault coverage while offers reduced storage requirements, shorter test application time, and smaller area overhead compared to weighted random approach. Due to the attractive features of mixed-mode approach, it has been used in proposed IC tester.

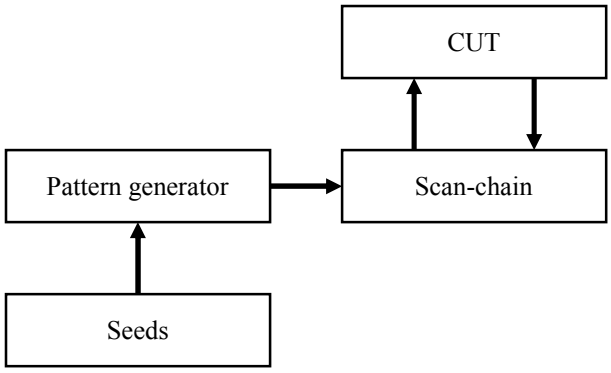

Fig. 1. Generalized scheme of mixed-mode technique

Generalized Linear Feedback Shift Register (GLFSR)

GLFSR are generalized LFSRs that are defined over Galois field *GF* (2^{δ}), $\delta \geq 1$. The general structure of the GLFSR (δ, *m*) is illustrated in Figure 2. The circuit under test (CUT) is assumed to have $n = (\delta \times m)$ inputs driven by the outputs of the GLFSR. A GLFSR (δ, *m*) have m stages $D_0, D_1, \cdots, D_{m-1}$, where each stage has δ storage cells of shift registers. Each shift shifts δ bits from one stage to the next stages.

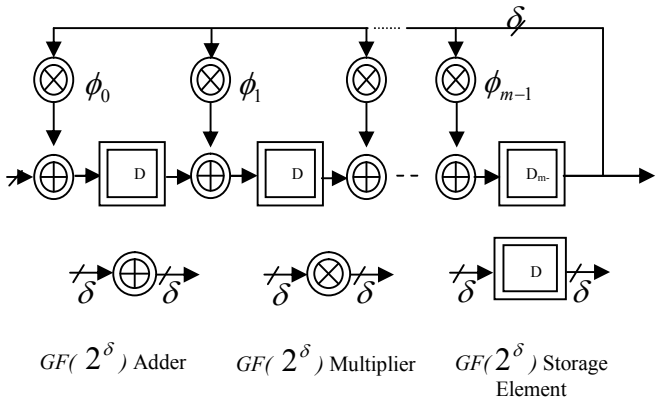

Fig. 2. The general structure of GLFSR [14]

The feedback polynomial of a GLFSR with *m* stage can be represented as

$$\phi(x) = \phi_0 + \phi_1 x + \phi_2 x^2 + \ldots + \phi_{n-1} x^{m-1} + x^m$$

The coefficients of the polynomial $\phi(x)$ are elements over *GF* (2^{δ}) and define the feedback connections. The i^{th} coefficient, ϕ_i multiplies the feedback input over *GF* (2^{δ}), which can be realized using only XOR gates. The GLFSR has different structure depending on the *"m"* and *"*δ*"* value. To generate patterns for a circuit of n inputs, a variety of GLFSR (δ, *m*) is available, where $(m \times \delta) \geq n.$ Different values of δ and m create different types of GLFSRs, capable of generating different types of patterns for the same *n*-input circuit. As the value of δ increases, the number of XOR gates needed to realize the generator increases. It has been shown that GLFSR is significantly more effective as a test pattern generator [14], providing better fault coverage than the standard LFSR. In the proposed IC tester Generalized Linear Feedback Shift Register (GLFSR) in place of LFSR has been used as pattern generator.

III. Proposed IC Tester

In this section we have proposed a complete design of IC tester. The mixed-mode testing approach has been implemented in the design. Here, GLFSR generated PRV is applied to a CUT to detect all the ETD faults and then deterministic test sets are generated using the same GLFSR to target the remaining HTD faults using compacted test data called seed. Therefore complete fault coverage can be achieved. Since the test algorithm is mixed-mode and pattern generator is GLFSR, it needs very less data storage requirement. So the cost of IC tester and testing time will remarkably reduce.

Architecture

The functional block diagram of the proposed conceptual IC tester is shown in Figure 3. Micro-UART, control unit, Pattern generator, Signature Analyzer (SA), Buffer Register (BR), Information Register (IR), and Random Access Memories (RAMs) are the main functional blocks of the IC tester.

Micro-URT: It consists of a transmitter and a receiver module. Data communication between personal computer (PC) and the SOC is performed through the UART. A user friendly interface is being developed for key-in the necessary information for IC testing.

Control Unit: It consists of a set of finite state machine (FSMs) and data paths. FSMs generate sequence of necessary controlling pulses for loading data in the memory and executing the test process of the circuit.

RAM: Necessary information for testing CUT such as test length of each test set, signature of the fault free CUT, seed of the GLFSR for random and deterministic test pattern generation are stored in memory modules (RAMs). Four RAMs named as test length storage RAM (TL_R), seed storage RAM for random test pattern generation (SD_R), seed storage RAM for deterministic test pattern generation (SDD_R) and signature storage RAM (SG_R) have been used.

Information register (IR): Test information for CUT such as number of primary input, primary outputs, number of test sets, number of deterministic seeds etc.

Buffer Register (BR): It is used to store the vectors generated from the GLFSR and the output response of the CUT.

Pattern Generator: It is a 4X8 bit GLGSR. The feedback connection of the GLFSR is based on the primitive polynomial.

Signature Analyzer (SA): The SA has similar structure of the PG except having two inputs, one is used to receive the output responses of the CUT and another is used to receive the scan-path responses of the CUT. Prior to start testing of a CUT, necessary test information is loaded from PC through micro-UART. The information register (IR), test length storage RAM (TL_R), seed storage RAM for random test pattern generation (SD_R), seed storage RAM for deterministic test pattern generation (SDD_R) and signature storage RAM (SG_R) are used to store the test data. Once data loading is completed, testing process is 'ON'. During testing process, test vectors are generated from the GLFSR and are loaded into the BR and are applied to the CUT. Output response of the CUT is captured into the BR and sent to the SA. At end of the test set, the generated signature is compared with that of a fault-free circuit of the same type (reference CUT). If the two signatures are the same, then the CUT is determined as fault-free, otherwise as faulty.

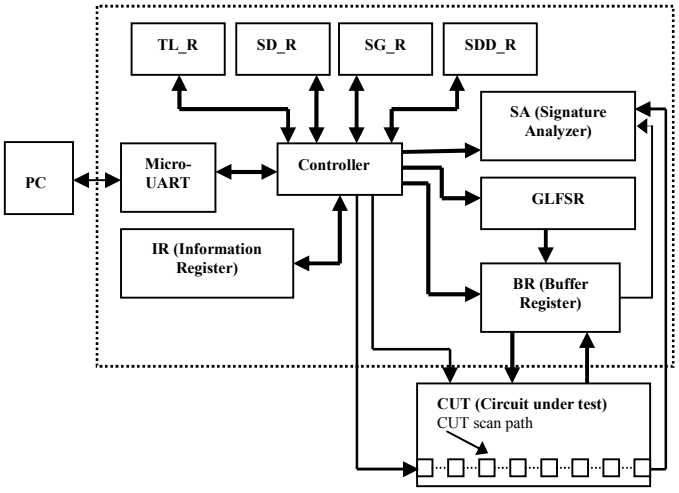

Fig. 3. Functional block diagram of the proposed IC Tester

Test Process

The operation of the IC tester has two phases: (a) load data in the IR and the RAMs (b) circuit test and retrieval of test result. Prior to start testing of a CUT the IR, TL_R, SD_R and SDD_R are loaded with appropriate information from PC through micro-UART. In the mixed-mode testing, pseudo-random testing approach is followed by deterministic testing approach. To start pseudo-random testing of the CUT, the controller reset the GLFSR, the BR, and the SA to zero and reads the test length, the seed and the signature from the TL_R, SD_R, and SG_R respectively. The GLFSR is initialized with the seed and generates PRV. The PRV is loaded into the BR and scan path (SP) and then applied to the CUT. The output response vectors of the CUT are captured into the BR and that of secondary output of the CUT into the SP. When the test vectors of the second test cube are loaded into BR and SP, output responses of the CUT due to the first test cube are shifted into the SA. The controller of the tester counts the number of test cubes of

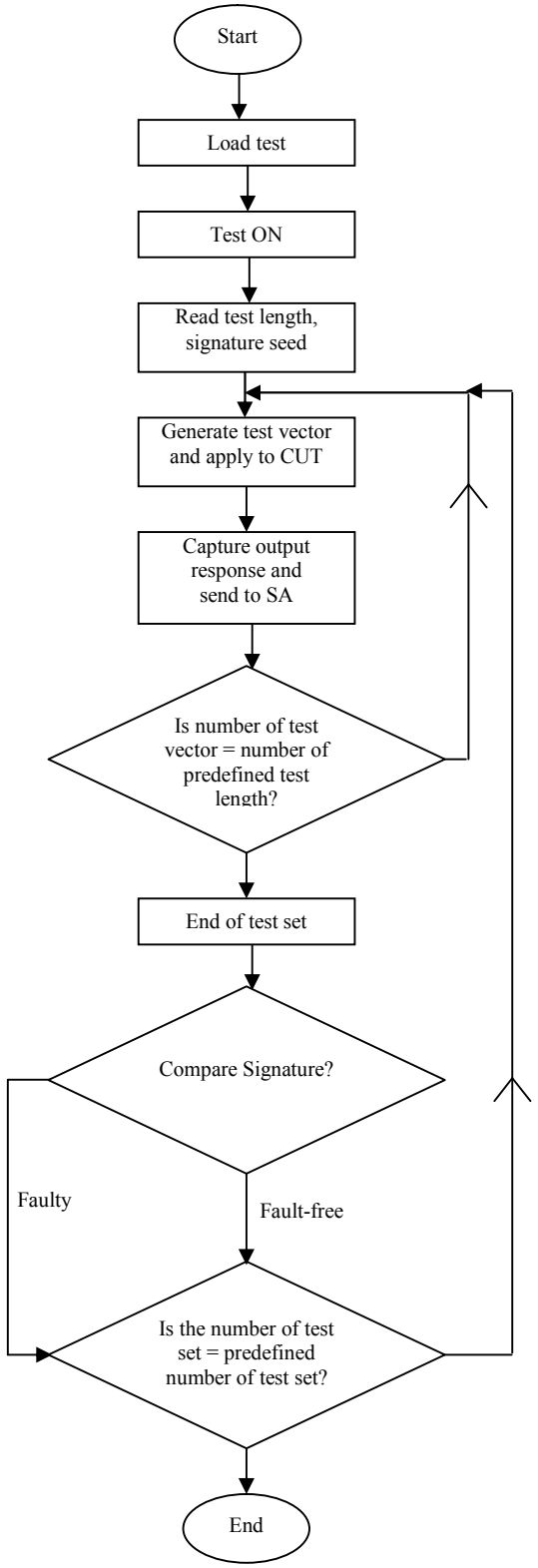

Fig. 4. GLFSR based mixed-mode Testing process

PRV applied to the CUT. The testing process continues until the test count equal to the predefined test length for the pseudo-random test. Once the pseudo-random test is

completed, the deterministic test starts. The controller reads the seed from the SDD_R and generates deterministic test cube by decoding the seed using the GLFSR. The test cube is applied to the CUT and the output response vectors are captured into the BR and send to the SA in the same fashion as that of the pseudo-random testing. The controller counts the number of deterministic test cubes applied to the CUT. When the number of the test cubes equals to the predefined number of deterministic test length then the generated signature is compared with that of the reference signature and the status of the CUT is determined as fault-free if the two signatures are the same otherwise as faulty. The flowchart of the test process is illustrated in Figure 4.

IV. Experimental Results

At first set of results of patterns from GLFSR and LFSR with different seeds and feedback polynomials have generated. Sample of such patterns are shown in Table 1. The patterns generated from GLFSR have significantly better randomness as shown in [14].

Table. 1. Sample of patterns generated from 8-bit LFSR and GLFSR based pattern generator.

LFSR	GLFSR
11111111	11111111
10111111	10101011
10011111	10111110
10001111	01010011
10000111	10000000
10000011	00100000
10000001	00001000
10000000	00000010
01000000	01111100
00100000	00011111
00010000	10010011
00001000	10110000
00000100	00101100
00000010	00001011
00000001	10010110
11000000	01011001

The fault simulation experiment will be conducted using digital fault simulator FSIM on ISCAS benchmark circuit.

V. Conclusion

Testing of IC with lower cost and reliable performance is an important issue in the today's semiconductor world. Review of different test technologies is done in this paper. It has been shown that mixed-mode approach is capable of testing IC with complete fault coverage using lower number of test vectors. It also has been shown that GLFSR generated patterns are more randomly distributed than LFSR which in turn result acceptable fault coveage using lower number of test vectors. We have presented the conceptual design of an IC Tester that can be used in IC testing effectively. The proposed design takes the advantages of the principle of the GLFSR and the mixed-mode testing approach. Since the proposed IC tester employed GLFSR based mixed-mode approach, it expected to overcome all the drawbacks of the traditional ATE-based IC testing. The design offers less control complexity, less test application time, less test data storage requirement and simple hardware implementation than any other existing IC Tester. The effectiveness of the proposed IC tester will be verified by conducting fault simulation experiments using ISCAS benchmark circuit. The proposed IC design can be realized as a system-on-a-chip (SoC) using hardware description language (HDL).

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